Multilevel Converter Based Intelligent Universal Transformer

TECHNICAL FIELD

[0001] The present invention relates generally to power conversion technology, and in particular to a multi-level converter based "all-solid-state" (electronic) universal transformer for power distribution systems.

BACKGROUND

[0002] Given the growing environmental, economic, and governmental concerns for building new power generation facilities, utilities continue to look for cost-effective ways to defer new power generation while meeting their customers' growing demand for electricity. In this environment, power producers need to mix and match their electrical services offering to meet the customers' changing requirements. While some major improvements (such as the introduction of grain-oriented core steel) have occurred in transformer technology from time to time, other developments in the areas of core, winding, insulation, and dielectric liquids have provided only incremental improvements in transformer technology. Thus, there is a continuing need for sophisticated transformer devices that can employ modern power electronics to improve transformer functionality.

[0003] There are two possible approaches for realizing such sophisticated devices with modern power electronics: the "hybrid" design and the "all-solid-state" design. The "hybrid" design is based on the integration of a conventional transformer with power electronics only on the secondary side of the transformer. The "all-solid-state" design, on the other hand, provides a fundamentally different and more complete approach in transformer design by using power electronics on the primary and secondary sides of the transformer. The power electronics on the primary side of the transformer provide a high voltage interface with the utility Alternating Current (AC) system and the power electronics on the secondary side of the transformer provide a low voltage interface with consumer applications.

[0004] All-solid-state (electronic) transformer technology can provide control over the shape and amplitude of output voltage waveforms and can, therefore, address many power quality problems. Electronic transformer designs can solve some shortcomings found

in conventional transformer technology, such as voltage drop under increasing load, "flat topped" voltage under saturation, harmonic sensitivity, containment requirements for oil spill, limited performance under Direct Current (DC) offset load unbalances, providing options for high-frequency AC, ability to convert single-phase service to three-phase for powering certain types of equipment, provide reactive compensation and so forth. In addition, this technology has the potential to lend itself to standardization of distribution transformers and to achieving other operational benefits like reduced weight and size, and reduced environmental concerns (e.g., by eliminating oil in the transformer, etc.).

[0005] One problem associated with all-solid-state transformers is the inability to provide isolation between the primary and secondary sides of the transformer. To convert two different voltage levels, it is often desirable to have transformer isolation to fully use the semiconductor switches in the transformer. One proposed solution is to modulate the input AC waveform by a power electronic converter to a high frequency square wave, which is then passed through a small, high-frequency transformer.

[0006] Several designs for solid-state power converters having high-frequency AC transformers have been proposed in the past. Some of those proposed structures can be used as building blocks for larger system structures. For example, a system structure can include multiple solid-state building blocks or modules having their inputs connected in series and their outputs connected in parallel. While such designs have some advantages (e.g., harmonic elimination, transformer isolation, reduction in size of magnetic materials, etc.), there are several drawbacks as well. For example, a problem inherent in such designs is the difficulty of ensuring that the input voltages balance among the different modules in the system structure. With device mismatching and without any active control, the input voltages among the different modules are unlikely to be maintained at the same voltage level. One solution may be to add a set of voltage balancing zener diodes, Metal Oxide Varistors (MOVs) or other passive voltage clamping methods. However, a typical passive voltage balancing element or clamping circuit consumes a large amount of power and is not practical in high-power applications.

[0007] Therefore, what is needed is multilevel converter-based intelligent, universal transformer that can interface directly to a power distribution system. The universal

transformer should allow for the series connection of an unlimited number of modern power semiconductor devices while maintaining proper voltage balance.

SUMMARY

[0008] The deficiencies of conventional systems and methods are overcome by the present invention, which provides a multilevel converter-based, intelligent universal transformer. The universal transformer includes back-to-back, interconnected, multi-level converters coupled to a switched inverter circuit via a high-frequency transformer. The input of the universal transformer can be coupled to a high-voltage distribution system and the output of the universal transformer can be coupled to low-voltage applications.

[0009] An embodiment of the present invention includes a power conversion device. The power conversion device includes a multilevel converter (e.g., a diode-clamped, multilevel converter) configurable to convert an input waveform having a first frequency into a second waveform having a second frequency. The second frequency is higher than the first frequency. A transformer is coupled to the multilevel converter and configurable to transform the second waveform from a first voltage level to a second voltage level. The first voltage level is higher than the second voltage level. A switched inverter circuit is coupled to the transformer and configurable to convert the transformed, second waveform into a third output waveform for use with a power application.

[0010] In some embodiments, the power conversion device includes a filter circuit coupled to the switched inverter circuit for smoothing the third output waveform into a substantially clean, sinusoidal waveform.

[0011] The multilevel converter of the present invention can be implemented using several different embodiments. In some embodiments, the multilevel converter further includes a first set of switches configurable to provide a multilevel, full-bridge converter; and a second set of switches coupled to the first set of switches and configurable to provide a multilevel, full-bridge inverter. The second set of switches are also configurable to provide a multilevel, half-bridge inverter. The switches can be high-voltage Integrated Gate Bipolar Transistors (IGBTs) for directly coupling the multilevel converter to a distribution voltage level.

[0012] An advantage of the universal transformer is that it is smaller in size than conventional copper-and-iron based transformers, yet provides enhanced power quality performance and increased functionality. The reduced size is the result of using a high-frequency transformer, which uses less magnetic materials.

[0013] Another advantage of the universal transformer is the use of modern power electronics to provide additional functionality, including: (1) voltage sag and outage compensation, (2) instantaneous voltage regulation, (3) capacitor switching protection, (4) harmonic compensation, (5) single-phasing protection, (6) DC output, and (7) variable frequency output (e.g., 50Hz, 60 Hz, 400 Hz, etc.).

BRIEF DESCRIPTION OF THE DRAWINGS

[0014] Figure 1 is a circuit diagram of a multilevel converter-based, intelligent universal transformer, in accordance with some embodiments of the present invention.

[0015] Figure 2A is a graph illustrating a line-to-line voltage waveform of a three-level converter, in accordance with some embodiments of the present invention.

[0016] Figure 2B is a circuit diagram illustrating a conventional three-phase nonlinear load, in accordance with some embodiments of the present invention.

[0017] Figure 2C is a graph illustrating a input current shaping using active, switched AC/DC conversion, in accordance with some embodiments of the present invention.

[0018] Figure 2D is a graph illustrating a output voltage and current waveforms under load variations, in accordance with some embodiments of the present invention.

[0019] Figure 3 is a circuit diagram of a basic three-level inverter, in accordance with some embodiments of the present invention.

[0020] Figure 4 is a circuit diagram of a three-phase multilevel converter adapted to be a front-end of the universal transformer in Figure 1, in accordance with some embodiments of the present invention.

[0021] Figure 5 is a circuit diagram of the front-end three-phase multilevel converter in Figure 4 but including a half-bridge inverter for high-frequency AC conversion, in accordance with some embodiments of the present invention.

[0022] Figure 6 is a circuit diagram of a multilevel solid state transformer circuit with a half-bridge front-end multilevel converter, a half-bridge multilevel inverter, a high-frequency transformer and a low voltage inverter, in accordance with some embodiments of the present invention.

[0023] Figure 7 is a circuit diagram of a five level inverter circuit, in accordance with some embodiments of the present invention.

[0024] Figure 8 is a circuit diagram of a three-phase front-end multilevel converter and three-phase multilevel inverter for high power applications, in accordance with some embodiments of the present invention.

[0025] Figure 9 is a block diagram of a converter/inverter control system, in accordance with some embodiments of the present invention.

[0026] Figure 10 is a block diagram of a universal transformer that has been modified to provide a DC output and a variable frequency output, in accordance with one embodiment of the present invention.

DESCRIPTION OF EMBODIMENTS

[0027] Figure 1 is a circuit diagram of a multilevel converter-based, intelligent universal transformer 100, in accordance with some embodiments of the present invention. The universal transformer 100 is an all-solid-state transformer comprising a single-phase, multilevel diode-clamped converter 102, a high frequency transformer 112 and a single-phase, DC-to-AC actively switched inverter 104. The input of the universal transformer 100 can be coupled to a distribution voltage level (e.g., 4160 Volts) and the output can be coupled to a low-voltage (e.g., 120 volts) consumer application. The multilevel converter 102 produces a high-frequency AC waveform which is fed into the high frequency transformer 112 for voltage level transformation from a first voltage level (e.g., 4160 Volts) to a second voltage level (e.g., 120 Volts). The transformed high-frequency AC waveform is then

rectified and converted from DC to AC by the low-voltage inverter 104 to produce a clean, sinusoidal waveform suitable for use in low-voltage applications. Including the multilevel converter 102 in the front-end of the universal transformer 100 to convert the input AC waveform into a high-frequency AC waveform, allows the use of the high-frequency transformer 112 to provide isolation and voltage transformation. A high-frequency transformer 112 is typically several orders of magnitude smaller in size than a conventional low frequency transformer because it uses less magnetic materials.

Overview of Multilevel Diode-Clamped Converter

[0028] The multilevel converter 102 includes a set of back-to-back, interconnected voltage-source converters 106 and 108, which are coupled via a pair of series connected DC bus capacitors 110-1 (C_1) and 110-2 (C_2). The DC bus capacitors 110 can be any DC voltage source (e.g., capacitor bank, battery) capable of maintaining voltage for a sufficient period of time to compensate for a disturbance or interruption.

[0029] The converters 106 and 108 include semiconductor switches 106-1 through 106-8 and 108-1 through 108-8, respectively. The switches can include Gate-Turn-Off (GTO) Thyristors, Integrated Gate Bipolar Transistors (IGBTs), MOS Turn-off Thyristors (MTOs), Integrated-Gate Commutated Thyristors (IGCTs), Silicon Controlled Rectifiers (SCRs) or any other semiconductor devices that have a turn-off capability. If the universal transformer 100 is to be connected directly to a distribution voltage level, then the switches 106 and 108 can be high-voltage IGBTs. With improved punch-through (PT) technology, high-voltage IGBTs (HV-IGBTs) are available at 3.3 kV, 4.5 kV, and 6.5 kV. Note that the number of voltage levels of the multilevel converters 106 and 108 can be increased or decreased without departing from the scope of the present invention.

[0030] Also included in the converters 106 and 108 are clamping diodes 107 and 109, respectively. The diodes 107 and 109 are for clamping the switch voltage to half the level of the DC bus voltage, V_{dc}, as described more fully below with respect to Figure 3.

[0031] In some embodiments, the converter 106 is configured as a multilevel, full-bridge converter that receives an AC voltage input and produces a DC voltage output. The full-bridge converter 106 has four pairs of switches 106 (e.g., S_{A1}-S_{A2}, S_{B1}-S_{B2}, S_{A1}'-S_{A2}', S_{B1}'-

S_{B2}·). The middle points *a-d* of the switch pairs are clamped to the middle point *N* (neutral point) of the split DC bus capacitors 110 or $V_{dc}/2$. In this configuration, each switch 106 blocks one capacitor 110 voltage level. For example, when both switches 106-1 (S_{A1}) and 106-2 (S_{A2}) turn on, the voltage across nodes *A* and *N* is $V_{dc}/2$, i.e., $V_{AN} = V_{dc}/2$. When both switches 106-5 (S_{A1}·) and 106-6 (S_{A2}·) turn on, the voltage across nodes *A* and *N* is $-V_{dc}/2$, i.e., $V_{AN} = -V_{dc}/2$. When both switches 106-2 (S_{A2}) and 106-5 (S_{A1}·) turn on, the voltage across nodes *A* and *N* is 0, i.e., $V_{AN} = 0$.

[0032] Note that the input voltage V_{AN} is an AC waveform with three levels: $V_{dc}/2$, 0, $-V_{dc}/2$. Similarly, for phase-b, the voltage between *B* and *N* is also a three-level AC waveform. The line-to-line voltage V_{AB} can have a total of five levels, as shown in Figure 2A.

[0033] A nonlinear load (such as the adjustable speed drive shown in Figure 2B) coupled to the output of the universal transformer 100 will produce a harmonic distorted load current, i_{La}, that tends to propagate back to the primary side of the high-frequency transformer 112. With proper switch control, however, the converter 102 shapes the input current, i_{SA}, to provide harmonic compensation. Switch control is described below with reference to Figure 9. Even if the load current, i_{La}, is harmonic distorted the input current i_{SA} is a clean, sinusoidal waveform in phase with the input source voltage, V_{AN}, as shown in Figure 2C. Also, note also that the actively switched, low-voltage inverter circuit 116 maintains a constant output voltage even if the load current, i_{La}, steps up or dumps out, as shown in Figure 2D.

[0034] If the universal transformer 100 is used in an application or system that requires outage compensation or short-term interruption protection, an energy storage device 118 can be coupled across the inputs of the inverter circuit 116 to ride-through these disturbances. When the input source voltage drops for a short period of time, the energy storage device 115 compensates for the deficit and maintains constant output voltage. The total period of compensation as a function of the amount of energy storage can be adapted as desired. The energy storage device 115 can include capacitor banks, ultra-capacitors, flywheels, batteries, or any other suitable storage media (or any combination thereof). In some embodiments, the energy storage device 115 can be switched into the inverter circuit

116 upon detection of a voltage sag and/or to provide outage compensation. In some embodiments, the duty cycle of the switches 106 can be controlled to ensure that the DC bus capacitors 110 maintain a constant voltage.

[0035] The universal transformer 100 provides the additional benefit of capacitor switch protection. In general, when using conventional transformers a power factor correction capacitor switching event produces a voltage transient to the nearby utility line. With the universal transformer 100, the voltage transient will not propagate to the secondary or load side because converters 106 and 108 can vary their conducting duty to accommodate changes in the input, such that the inverter 104 would not see a high-side voltage transient.

[0036] Figure 3 is a circuit of a basic three-level inverter 300, in accordance with some embodiments of the present invention. The three-level inverter 300 will be used to describe the operation of the first half (switches S_{a1}, S_{a2}, $S_{a1'}$, $S_{a2'}$) of the multilevel converter 108 in Figure 1, which in some embodiments is configured as a three-level inverter.

[0037] Referring to the inverter 300, the DC bus voltage, V_{dc}, is split into three voltage levels by two series-connected bulk capacitors 302-1 (C_1) and 302-2 (C_2). The middle point of the capacitors 302, N, can be defined as a neutral point (e.g., ground). The output voltage, V_{AN}, has three states: $V_{dc}/2$, 0, and $-V_{dc}/2$. For voltage level $V_{dc}/2$, switches 304-1 (S_1) and 304-2 (S_2) are turned on. For voltage level $-V_{dc}/2$, switches 304-3 ($S_{1'}$) and 304-4 ($S_{2'}$) are turned on. For a 0 voltage level, 304-2 (S_2) and 304-3 ($S_{1'}$) are turned on.

[0038] Components that distinguish the inverter 300 from a conventional two-level inverter are clamping diodes 306-1 (D_1) and 306-2 ($D_{1'}$). The clamping diodes 306 clamp the switch voltage to half the level of the DC bus voltage, V_{dc}. When both switches 304-1 (S_1) and 304-2 (S_2) turn on, the voltage across nodes A and 0 is V_{dc}, i.e., $V_{A0} = V_{dc}$. In this case, diode 306-2 ($D_{1'}$) balances out the voltage shared between switches 304-3 ($S_{1'}$) and 304-4 ($S_{2'}$) with switch 304-3 ($S_{1'}$) blocking the voltage across capacitor 302-1 (C_1) and switch 304-4 ($S_{2'}$) blocking the voltage across 302-2 (C_2). Note that output voltage V_{AN} is an AC waveform, and V_{AO} is a DC waveform. The maximum voltage level for V_{A0} is V_{dc}, and the maximum voltage level for V_{AN} is $V_{dc}/2$. The difference between V_{AN} and V_{A0} is the voltage across C_2, which is $V_{dc}/2$. If an output is added between nodes A and 0, then the inverter 300

can be configured as a DC/DC converter having three output voltage levels: V_{dc}, $V_{dc}/2$, and 0, as described with respect to Figure 10.

Overview of Low-Voltage Inverter

[0039] Referring again to Figure 1, the low-voltage inverter 104 includes a diode bridge 114, a DC bus capacitor 120 and an actively switched inverter circuit 116. Under normal operation, an AC waveform is received from the secondary side of the high-frequency transformer 112 and rectified to a DC waveform by the diode bridge 114. The DC waveform charges the DC bus capacitor 120 to provide a stable voltage source for the switched inverter 116. The switched inverter circuit 116 includes semiconductor switches 116-1 through 116-4 (S_1-S_4) that can be rapidly switched (e.g., at approximately 20,000 to 40,000 Hz) to convert the DC voltage stored at the DC bus capacitor circuit 120 to a synthesized AC waveform. The DC bus capacitor 120 can be any DC voltage source (e.g., capacitor bank, battery) capable of maintaining voltage for a sufficient period of time to compensate for a disturbance or interruption. In some embodiments, the number of switches 116 and their rate of switching may be different from the exemplary values of the embodiment shown in Figure 1.

[0040] The switched inverter 116 can have many different inverter circuit topology options. For example, the inverter 116 can be a half bridge-based inverter, which relies on capacitor-split sources and phase-leg switches to produce PWM (pulse width modulated) output. The inverter 116 can also be a cascaded inverter as described in U.S. Patent No. 5,642,275, which is incorporated by reference herein in its entirety.

[0041] In some embodiments, a filter circuit 118 is coupled to the output of the inverter 116 (nodes e and f) for smoothing the output high frequency AC waveform. By adding the filter circuit 118 to the output, the AC output waveform is sinusoidal with substantially reduced ripple. In some embodiments, the filter circuit 118 includes an inductive element L_f coupled to a shunt capacitance C_f to form a low pass filter. The series inductor L_f and shunt capacitor C_f pair can also be split into two stages of series-inductor and shunt-capacitor pairs cascaded to form a higher order low pass filter. In other embodiments, the inductive element L_f can be coupled directly to the utility line without the need of the shunt capacitor C_f. Note that other combinations of passive and/or active devices can be

coupled to the switched inverter 116 for smoothing the output waveform using well-known filter design techniques.

[0042] The basic operation of the inverter 116 is to switch the S_1-S_2 and S_3-S_4 pairs in an alternating fashion so that the inverter 116 output voltage is an alternating chopped DC voltage. The filter 118 smoothes the chopped DC voltage into a clean, sinusoidal waveform. The switches 116 can be controlled by an external controller using either analog or digital control signals in a manner commonly known to one of ordinary skill in the art. For example, the states of switches 116 can be controlled using pulse-width modulation (PWM) techniques. In PWM, the width of pulses in a pulse train is modified in direct proportion to a small control voltage. By using a control waveform of a desired frequency as a control voltage, it is possible to produce a waveform whose average voltage varies sinusoidally in a manner suitable for driving the switches 116. An embodiment of a pulse-width modulation inverter control circuit is described below with respect to Figure 9.

[0043] If the universal transformer 100 is used in an application or system that requires outage compensation or short-term interruption protection, an energy storage device (not shown) can be coupled across the inputs of the low-voltage inverter 104 (e.g., in parallel with the DC Bus capacitor 120) to mitigate disturbances. When the input source voltage drops for a short period of time, the energy storage device compensates for the deficit and maintains constant output voltage. The total period of compensation as a function of the amount of energy storage can be adapted as desired. The energy storage device can include capacitor banks, ultra-capacitors, low-speed flywheels, batteries, or any other suitable storage media (or any combination thereof). In some embodiments, the energy storage device can be switched into the universal transformer 100 upon detection of a voltage sag and/or to provide outage compensation.

Other Embodiments of the Multilevel Converter

[0044] Figure 4 is a circuit diagram of a three-phase multilevel converter 400, in accordance with some embodiments of the present invention. The multilevel converter 102 in Figure 1 can be replaced with the three-phase multilevel converter 400.

[0045] In this embodiment, an additional branch of switches 402 (S_{C1}, S_{C2}, $S_{C1'}$, and $S_{C2'}$) is added to the converter 400, such that the input of the converter 400 can be directly tied to a three-phase distribution source. The three-phase converter 400 allows power conversion directly from the three-phase source to a single-phase output, while reducing unbalance loading among the three phases. The basic switch control of the converter 400 is similar to the multilevel converter 102, except for the additional branch of switches 402, which must be switched as well. Switch control for a three-phase input is further described with respect to Figure 9.

[0046] Figure 5 is a circuit diagram of a three-phase multilevel converter 500 but including a front-end converter 502 coupled to a half-bridge inverter 504 for high-frequency AC conversion, in accordance with some embodiments of the present invention. The converter 500 not only reduces the number of devices and components, but also reduces the transformer insulation requirement because its output voltage is only half that produced by a full-bridge inverter. If the voltage source is tied from line to neutral, it is possible to further reduce the parts count by connecting the source neutral to the middle point N of the capacitor stack (C_1, C_2). This circuit change reconfigures the front-end converter 502 into a half-bridge converter.

[0047] Figure 6 is a circuit diagram of a multilevel solid state transformer circuit 600 with a half-bridge front-end multilevel converter 602, a half-bridge multilevel inverter 604, a high-frequency transformer 606 and a low voltage inverter 608, in accordance with some embodiments of the present invention. In the circuit 600 as shown, the low voltage inverter includes a low-voltage side diode-bridge 610. If the low-voltage side diode-bridge 610 is replaced with an IGBT-based full-bridge converter, then the transformer 600 is symmetrical with the front-end multilevel converter 602 at the high-voltage side and a full-bridge converter at the low-voltage side, thus enabling bi-directional power flow. In some embodiments a filter circuit 612 is coupled to the input of the front-end multilevel converter 602 to smooth the input AC waveform prior to conversion. The front-end multilevel converter 602 is a five-level, diode-clamped converter, which includes four DC bus capacitors. The operation of the front-end multilevel converter 602 is further described with respect to Figure 7.

[0048] Figure 7 is a circuit diagram of a five-level, diode-clamped converter 700 in accordance with some embodiments of the present invention. The converter 700 includes a DC bus 702 comprising four DC bus capacitors, C_1, C_2, C_3, and C_4. For the DC bus voltage, V_{dc}, the voltage across each capacitor is $V_{dc}/4$, and the voltage stress on each device will be limited to one capacitor voltage level, $V_{dc}/4$, by clamping diodes D_1, D_1', D_2, D_2', D_3 and D_3'. To explain how the staircase voltage 704 is synthesized, the neutral point, N, is considered as the output phase voltage reference point. There are five switch combinations to synthesize five level voltages across A and N.

[0049] For voltage level $V_{AN} = V_{dc}/2$, turn on all upper switches, S_1 through S_4. For voltage level $V_{AN} = V_{dc}/4$, turn on three upper switches, S_2 through S_4 and one lower switch, S_1'. For voltage level $V_{AN} = 0$, turn on two upper switches, S_3 and S_4, and two lower switches S_1' and S_2'. For voltage level $V_{AN} = -V_{dc}/4$, turn on one upper switch, S_4, and three lower switches, S_1' through S_3'. For voltage level $V_{AN} = -V_{dc}/2$, turn on all lower switches, S_1' through S_4'. Four complementary switch pairs exist in each phase. The complementary switch pair is defined such that turning on one of the switches will exclude the other from being turned on. In this example, the four complementary pairs are (S_1, S_1'), (S_2, S_2'), (S_3, S_3'), and (S_4, S_4'). Although each active switching device is only required to block a voltage level of $V_{dc}/(m-1)$, the clamping diodes should have different voltage ratings for reverse voltage blocking, where m represents the number of distinct voltage levels produced by the converter. Note that m=5 for a five level converter, so the voltage level stress for each switch is $V_{dc}/4$. Likewise, m=3 for a three-level converter, so the voltage level stress for each switch is $V_{dc}/2$.

[0050] When the lower switches S_2'-S_4' are turned on, D_1' needs to block three capacitor voltages, or $3V_{dc}/4$. Similarly, D_2 and D_2' need to block $2V_{dc}/4$, and D_3 needs to block $3V_{dc}/4$. Assuming that each blocking diode voltage rating is the same as the active switch voltage rating, the number of diodes required for each phase will be $(m-1)\times(m-2)$.

[0051] In practice the off-the-shelf high-frequency magnetic materials used to construct the high-frequency transformer used in the described embodiments may be limited in size and power. Such limitations, however, may not be sufficient for certain power applications. The largest off-the-shelf size ferrite EE core with 80 mm or 90 mm length may

be designed for up to 20 kW depending on the switching frequency. Although it is possible to have custom-made magnetic cores for higher power applications, the cost to make such cores may be prohibitively expensive unless there is a large quantity order. Figure 8 shows a possible option with a three-phase multilevel inverter to triple the power level.

[0052] Figure 8 is a circuit diagram of a front-end multilevel converter 800, in accordance with some embodiments of the present invention. The converter 800 includes a three-phase multilevel converter 802 and a three-phase multilevel inverter 804. Note the output of the three-phase multilevel inverter 804 can be coupled to a three-phase high-frequency transformer or three single-phase transformers (not shown). A three-phase high-frequency transformer typically has one core with three sets of windings. However, the core can be separated into three sets with their own independent windings. Further, the three-phase high-frequency transformer windings can be connected in a Y or Δ configuration for either the primary or secondary sides of the transformer.

[0053] Figure 9 is a block diagram of a converter/inverter control system 900 for controlling a converter or inverter 902, in accordance with some embodiments of the present invention. The feedback control system 900 includes a processor 906 (e.g., microcomputer, digital signal processor), a scaling factor circuit 908, a set of gate drivers 910 and a command interface 912. The processor further includes a pulse width modulator 914, a controller 916 and memory 918 (e.g., DRAM, SRAM, and/or Flash Memory). The scaling factor circuit 908 and the gate drivers 910 isolate control signals from the power.

[0054] In operation, the processor 906 compares a command voltage V_{ref} and a scaled feedback output signal V_{sense} to determine an error signal V_{error}. The feedback signal, V_{sense}, is taken from the output of the converter/inverter 902. The error signal V_{error} is received by the controller 916, which applies a proportional (P), proportional-integral (PI), or proportional-integral-differentiator (PID) function to the error signal so as to generate a smooth duty cycle signal, $d(t)$. Note that in a typical application, either a load (e.g., adjustable speed drive) or another converter/inverter 904 is coupled to the output of the converter/inverter 902.

[0055] The duty cycle of each switch is computed by the processor 906 using one or more computer programs or gate pattern logic stored in memory 918. The resulting duty cycle signal, $d(t)$, is then sent to the pulse width modulator 914 (PWM), which generally

includes a set of voltage comparators. In some embodiments, one comparator is used for each pair of switches. For example, the switch pair S_1-S_2 in the actively switched inverter 104 (Figure 1) can be controlled by a first comparator and the switch pair S_3-S_4 can be controlled by a second comparator. The PWM signals are then fed into the gate drivers 910 to turn the switches in the converter/inverter 902 on or off. The number of switches in the converter/inverter 902 depends on how many voltage levels and phases are to be controlled.

[0056] The control voltages *d(t)* (and therefore the output pulse width) can be varied to achieve different frequencies and voltage levels in any desired manner. For example, the processor 906 can implement various acceleration and deceleration ramps, current limits, and voltage-versus-frequency curves by changing variables (e.g., via the command interface 912) in control programs or gate pattern logic stored in memory 918.

[0057] If the duty cycle *d(t)* is greater than the voltage level of a reference waveform (e.g., a triangular waveform) at any given time t, then the PWM circuit 914 will turn on the upper switches (e.g., switches S_1 and S_2) of inverter 104 and turn off the lower switches (e.g., switches S_3 and S_4) of the inverter 104. For a three-phase PWM inverter embodiment (e.g., the embodiment shown in Figure 8), three single-phase control circuits can be used with control voltages comprising sinusoidal waveforms shifted by 120 degrees between phases using techniques well-known in the art.

[0058] In some embodiments, the control system 900 includes a detection circuit configured to detect when the input power source has a missing phase or is running under a single-phase condition and to generate control signals to be used by the command interface 912 to shut off the switches in one or more phase-legs of the universal transformer.

[0059] Figure 10 is a block diagram of a universal transformer 1000 that has been modified to provide a DC output and a variable frequency output, in accordance with one embodiment of the present invention. The universal transformer 1000 includes a multilevel converter 1002 coupled to a low-voltage inverter circuit 1008 (e.g., 120 Volts @ 60 Hz) via a high-frequency transformer 1004. The universal transformer 1000 is the same as the universal transformer 100 shown in Figure 1, except for the addition of a second low-voltage inverter circuit 1006, which provides a 400 Hz output. The second inverter 1006 takes it input from across the DC bus (nodes a and b). Note that other inverter circuits having

different output frequencies (e.g., 50 Hz) can be added to the inverter 1008 in a similar manner to provide a variable frequency output.

[0060] Additionally, the universal transformer 1000 can be modified to provide one or more DC output levels by coupling a DC/DC converter 1010 across the DC bus of inverter 1008 (nodes a and b). In some embodiments, the DC/DC converter 1010 can be a multilevel DC/DC converter for providing a variety of different DC voltage levels.

[0061] The foregoing description, for purpose of explanation, has been described with reference to specific embodiments. However, the illustrative discussions above are not intended to be exhaustive or to limit the invention to the precise forms disclosed. Many modifications and variations are possible in view of the above teachings. The embodiments were chosen and described in order to best explain the principles of the invention and its practical applications, to thereby enable others skilled in the art to best utilize the invention and various embodiments with various modifications as are suited to the particular use contemplated.